PM-1100
Core Memory
Manual

Plessey
Microsystems

PM-1100
CORE MEMORY MANUAL

PLESSEY MEMORIES, 1674 McGaw Avenue, Santa Ana, California 92707

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1.0 SCOPE

This manual provides information to familiarize the users of PM-1100 memories manufactured by Plessey Memories Incorporated, 1674 McGaw Avenue, Santa Ana California 92705, with its design and modes of operation. It assumes the reader to be familiar with the 3D-3Wire concept of core memory design.

2.0 GENERAL DESCRIPTION

PM-1100 is a 8192x16 bit 3D-3Wire core memory housed in one printed curcuit board and dedicated to operate in Digital Equipment Corporation's PDP-11 computer. The PM-1100 memory is fully plug-in compatible with the DEC MM11-F, DEC MM11-E and all the standard peripheral device control units used in the PDP-11 computer.

2.1 Reliability

PM-1100 is designed around the best electronic components and integrated curcuits available in today's technology incorporating state-of-the-art high reliability design concepts. The magnetic cores used are housed in a 8192x16 bits planar core array, designed and manufactured by Plessey Memories Inc. and used extensively in the computer industry.

2.2 Maintenance

Each memory is thoroughly tested and exercised under absolute worst case conditions before they leave the factory; however, if the memory were to malfunction while being used, it must be returned to the factory for repair. The information contained in this manual may be used by qualified technicians to isolate problem areas and replace defective components, if necessary. Reference Figure 1 Assembly Drawing and Figure 2 Schematic.

Although this type of on-site repair may save some downtime on the computer, it is strongly recommended that the memory be sent back to the factory for repair to ensure that the unit is tested to the specified requirements before being used again. This also obviates the possibility of the computer being damaged by a faulty memory.

2.3 Mechanical

Two PM-1100 memories (16384x16 bits) mounted on a special chassis, provided by Plessey Memories Inc., physically fits into the space used by one DEC MM11-F (4096x16 bits) or any of the standard DEC device control units.

2.3 (Cont.)

This convenient, compact packaging feature enables the maximum memory capacity of 28672x16 bits of the basic PDP-11 computer to be housed in the main chassis+ rather than using an extended chassis, which would have been necessary, if only DEC MM11-F memory units were to be used. The PM-1100 (16K) assembly is 2.2" x 16.5" x 10.0", while the basic PM-1100 printed curcuit board measures 14.3" x 8.9" x .8".

2.4 Environment

PM-1100 memory is capable of sustained operation in the basic PDP-11 chassis or an extended chassis thereof over a temperature range of 0°C to +50°C and up to 90% RH (without condensation).

2.5 Power Requirements

PM-1100 memory uses two power supplies, +5V and -15V, as the DEC memory. The power requirement for one basic PM-1100 assembly is listed below.

Power Supply	Standby	Non-Interleaved Operation	Continuous Interleaved Operation
+5V ± 5%	2.0	3.0	5.5
-15V ± 2%	.15	6.5	11.0

3.0 TECHNICAL FEATURES

3.1 Capacity — 8192x16 bits (basic PM-1100)
16384x16 bits (one memory assembly)

3.2 Access Time — Less than 400ns

3.3 Cycle Time — 950ns

NOTE: Memories may be accessed with less than 600ns cycle time when interleaved. Refer Appendix A for details on the interleave option.

+The necessity of having an adequate power supply in the main chassis when housing 28K of memory in it, cannot be overemphazied.

3.4	Interface	The memory interfaces with the central processor, other memories and peripheral device controllers via the *Unibus (See Appendix A).
3.5	Addressing	The memory in direct interface with the unibus, receives the full complement of a 18-bit address available on the latter. The least significant bit, AØØ is used for byte selection when operating in Byte Mode. AØ1 through A13 are used for locating a word within the 8192 word memory, while A14 through A17, together with A13, are used for selecting the memory.
3.6	Memory Selection	As explained in the Appendix A, each device attached to the unibus examines the address lines when the unibus master flags its desire to communicate with a device, but only the device with the unibus address falling within its address block will respond. Each memory is strapped to respond to a 8192 word address block with starting addresses 0, 4096, 8192, 16384 and 24576, using addresses A13 through A17. Address strapping is implemented using an Address Strapping Plug supplied by Plessey Memories Inc. The usage and details of the address strapping plugs are given in Figure 5 of Appendix A.

3.7 Operating Modes

The memory can operate in the following modes:

Read - Restore	DATI
Half-Cycle Read	DATIP
Clear - Write	DATO
Read - Restore Bytes/Clear-Write Byte 0	DATOB Ø
Read-Restore Byte 0/Clear Write Byte 1	DATOB 1

---

*Unibus is a registered trademark of Digital Equipment Corporation.

Mode selection is done by two control lines on the unibus in conjunction with the AØØ line. The various modes may be exercised in any sequence and combination, with one exception. A DATIP mode operation has to be followed by a DATO or DATOB operation. The internal control logic of the memory will always convert the mode, following a DATIP to a half cycle write operation if that mode was not requested next.

3.8 Interleave Option

The memory is capable of interleaved operation. The details are given in Appendix A.

4.0 THEORY OF OPERATION

PM-1100 memory system may be broadly divided into four basic subdivisions.

a. Timing and control circuitry..

b. Planar core array.

c. X & Y current drive circuitry.

d. Data Loop circuitry.

4.1 Timing and Control Circuitry

The memory which can only act as a slave of the unibus (See Appendix A) receives commands ,address and data information on the unibus. The internal circuitry of the memory responds to these signals in the following sequence (Figure 3)

a. The address information on the unibus is examined.

b. If the unibus address does not fall within the address block to which the memory is strapped it continues to remain in its non-cycling state. Otherwise the mode information on the unibus is decoded and at the occurrence of the MSYN sent by the bus master, the memory raises an internal flag MSEL indicating it is busy, timing signals necessary to perform the required mode are generated and simultaneously the address bits ØØ thru 13 are stored. If the required mode happens to be a WRITE operation then the data bits are also stored at the same time.

c. The memory, if cycling, responds to the MSYN from the bus master by a SSYN acknowledging the MSYN and indicating its presence. Bus master removes the MSYN once SSYN is sent by the memory. In turn the memory removes its SSYN. When both MSYN and SSYN are removed from the unibus , the latter is free and may be taken over by a device. But the memory is still cycling and it cannot be accessed until it stops cycling.

d. Once the memory completes cycling it removes its internal busy flag MSEL and is ready for communication with any device which becomes the unibus master.

4.1.1 Modes Of Operation

Two control lines CØ and C1 in conjunction with AØØ address line select one out of five modes of operation as shown in Figure 4).

4.1.1.1 Read-Restore (Data-In) (Figure 5)

This is conventional Read-Restore mode where the data read out of (and thus destroyed from) the core during the first half of the memory cycle at a selected address is automatically restored in the core at the same location during the second half of the cycle without additional commands from the unibus master.

4.1.1.2 Clear-Write (Data-Out)

This is also a conventional clear-write mode where core at a selected location is first cleared and new data is written during the second half of the cycle.

4.1.1.3 Read Half-Cycle (Data-In, Pause)

Under certain circumstances, the unibus master would want to read out a given location and may want to write new data back at that location. The unibus master would also need some time to examine the data it had read out of the memory and decide on what new data has to be rewritten back in the memory.

4.1.1.3 (Cont.)

In the DATIP mode the memory presents the data in core to the unibus during the first (READ) half of the cycle and stops cycling indefinitely until the unibus master presents new data to the memory and issues a command to write that data into that location. The logic circuitry built into the memory ensures the operation following a DATIP is always a DATO or a DATOB operation.

4.1.1.4 Clear-Write Byte (Data-Out, Byte)

The unibus master under certain circumstances may wish to write new data into only one of the bytes at a given location. The memory executes this request by the first reading both bytes while the other byte is restored during the write half of the cycle. The address line AØØ selects one of the two bytes during byte operation.

4.2 Planar Core Array

The field proven Plessey Core Array 700017-101 is used in the PM-1100 memory. This array is of 3D-3Wire organization and uses 18 mil lithium/nickel core. The X:Y aspect ratio of the array is 128:64. The X dimension carries 8 drives and 16 sinks with two diodes per line while the Y dimension has 8 drives and 8 sinks with the same number of diodes per line. Each sense/inhibit line threads through the full complemtnt of 8192 cores. The sense/inhibit lines are terminated with two 150Ω resistors to ground at the sense amplifier and 75Ω at the inhibit switch. The array is driven with positive Y and negative X current during a Read operation and with negative Y, positive X and negative inhibit current during the Write Operation. This arrangement of the core array permits a "shared drive" scheme (Figure 6) to be used in the PM-1100 system minimizing the number of components used and thus improving the system reliability. See Figure 7 for stack pin function.

4.3 X & Y Current Drive Circuitry

Figure 8 depicts the X & Y current drive scheme used in the PM-1100 memory system. The circuitry may be broadly divided into four basic sections;

a. Current Regulator

b. Address Registers

c. Address Decoders

d. Current Switches.

4.3.1 Current Regulator

The current regulator section consists of two regulated current sources +STAB and -STAB. Both sources drain current from +5V supply and sink to -15V supply. The +STAB source is used to drive positive current into the stack required by Y-read and X-write operations. The regulation of this source is done at the +5V end of the drive path. The -STAB source drives negative currents from the stack during X-read and Y-write operations and is regulated at the -15V end of the drive path. Both +STAB and -STAB sources are regulated against a common reference voltage so that the X and Y currents in both the Read and Write operations remain in balance once they have been set to be balanced at any current. The common reference voltage is controlled by a sensistor which changes its resistance with temperature and causes the drive currents to be "compensated" for the changes in ambient temperature. The drive current is a factory set level of 400 ma.

4.3.2 Address Registers

The address registers store the address information on lines AØØ thru A13 of the unibus when they are presented to the memory at the beginning of a cycle. The address registers retain this addressing information until the beginning of another Read operation in the memory. As explained in Appendix A, this is one of the features which permits interleave operation of memories.

4.3.3 Address Decoders

The address decoders converts the address information in the address registers to actual core locations as seen by the memory. However, the address bit ØØ is not being used for location selection and is used only for selection of either the Byte Ø or Byte 1 during a DATOB operation. The address bits Ø2, Ø3 and Ø8 are decoded to select 1 of 8 Y-Drive switches while the address bits Ø4, Ø5 and Ø6 are decoded to select 1 of 8 Y-sink switches.

4.3.3 (Cont.)

1 of 8 X-Drive switches are selected by decoding address bits 11, 12 and 13 and the address bits Ø1, Ø7, Ø9 and 1Ø select 1 of 16 X-Sink switches. When the system is wired for interleave operation (Appendix A) the address bits Ø1 and 14 are transposed and in this mode of operation address bits 14, Ø7, Ø9 and 1Ø select the X-Sink switches.

4.3.4 Current Switches (Figure 9)

The current switches may be functionally separated into two categories, the Drive Switches and the Sink Switches. However, all the current switches (including the inhibit switches) used in the PM-1100 system are similar in electrical design. All of them are floating switches using a transformer-coupled transistor as the switch. The decoders when activated by the timing pulses draw current through the primary of the transformer in the selected switch. This primary current induces current in the secondary connected across the base and the emitter of the transistor switching the transistor ON.

One unique feature of the drive organization is the "shared drive" scheme (Figure 4). The same current switch that drives Y-read current also drives X-write current. Also one current switch drives both Y-write and X-read currents . Thus by time sharing one current switch between the X & Y dimensions PM-1100 memory uses only half the drive switches used by a conventional design approach to drive an identical size core array.

4.4 Data Loop Circuitry (Figure 10)

The Data Loop circuitry consists of the receiver, register, sense amplifier, inhibit and the output buffer. The timing signals required for the Data Loop are generated in the Timing and Control.

A DATO cycle (Clear/Write) requires resetting (reset 0L and 1L) the data register, then strobing (Load 0L and 1L) the data in from the Unibus. During the clear cycle the selected address in the memory is cleared. (Setting cores to zero). During Write, the selected address receives a half select current in both the X and Y axis, thereby switching the core to a "1". If a "0" is to be written into a selected core location the Inhibit Driver is turned on. This opposes the Y write current and therefore leaves the core in the "0" state.

A DATI cycle (Read/Restore) requires reading out of a selected core location and restoring the same information. During the read cycle the data register is reset. The sense amplifier is set to a specific threshold and when the strobe is applied approximately during the peak of a "1" signal it will set the data register. The S.A. strobe is a factory adjustment and is set approximately 340ns from BUS MSYL. A "0" signal will not exceed the threshold voltage during the strobe time and therefore leave the data register in the reset state. The restore cycle is similar to the write portion of the DATO cycle. The strobe adjustment is critical and should only be changed when absolutely necessary. The threshold voltage to the sense amplifier is approximately 18 millivolts and is generated by a voltage divider network connected to +5V.

The DATA OUT H signal gates the data register flip-flop onto the Unibus thru the open collector bus driver.

The inhibit driver is a floating transformer coupled transistor switch. The primary is driven from a integrated circuit. Primary current flows in the transformer when the output from the data register (data "0") and the inhibit timing signal are high at the input to the gate.

5.0 INSTALLATION (FIGURE 10)

Following steps are listed as a guidance in installing PM-1100 (8192x16) or PM-1100 (16384x16) memory assemblies in the PDP 11/20 Computer.

INSTRUCTIONS

1. Remove from shipping container.

*2. Remove the memory retaining hardware in one of the two 8K memory modules and searate the 8K memory module from the rest of the assembly.

3. Set the OFF-POWER-PANEL LOCK switch on the front panel to the OFF position. Pull unit from cabinet to maximum travel and lock.

4. Remove protective top cover. Lower the memory assembly into the first vacant slot in the unit with the memory mounting bracket uppermost parallel to the width of the chassis and components facing the operator. Secure the memory mounting bracket in place with captive hardware (View A-A).

5. Tilt-and-with unit as shown in vertical position (View B-B) and remove bottom cover.

6. Plug the unibus paddle board of the memory assembly in place of the terminator board in the unibus connector on the adjacent chassis and plug the terminator board in the unibus connector of the memory assembly. (Note: The term "terminator board" in STEP 6 shall read as "extender cable paddle board" when installation is done in an extended chassis unit).

7. Plug the power paddle board into the power connecter (View B-B).

*8. Plug the 8K memory module removed in Step 2 back into the memory assembly with the components on both 8K modules facing in the same direction and secure in place using memory retaining hardware.

9. Place the bottom cover back and secure in position. Tilt the unit back to the horizontal position (View A-A).

10. Place the top cover back and secure in position. Depress side locks and slide unit into cabinet.

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* Steps 2 and 8 are to be omitted when installing a PM-1100 (8Kx16) memory.

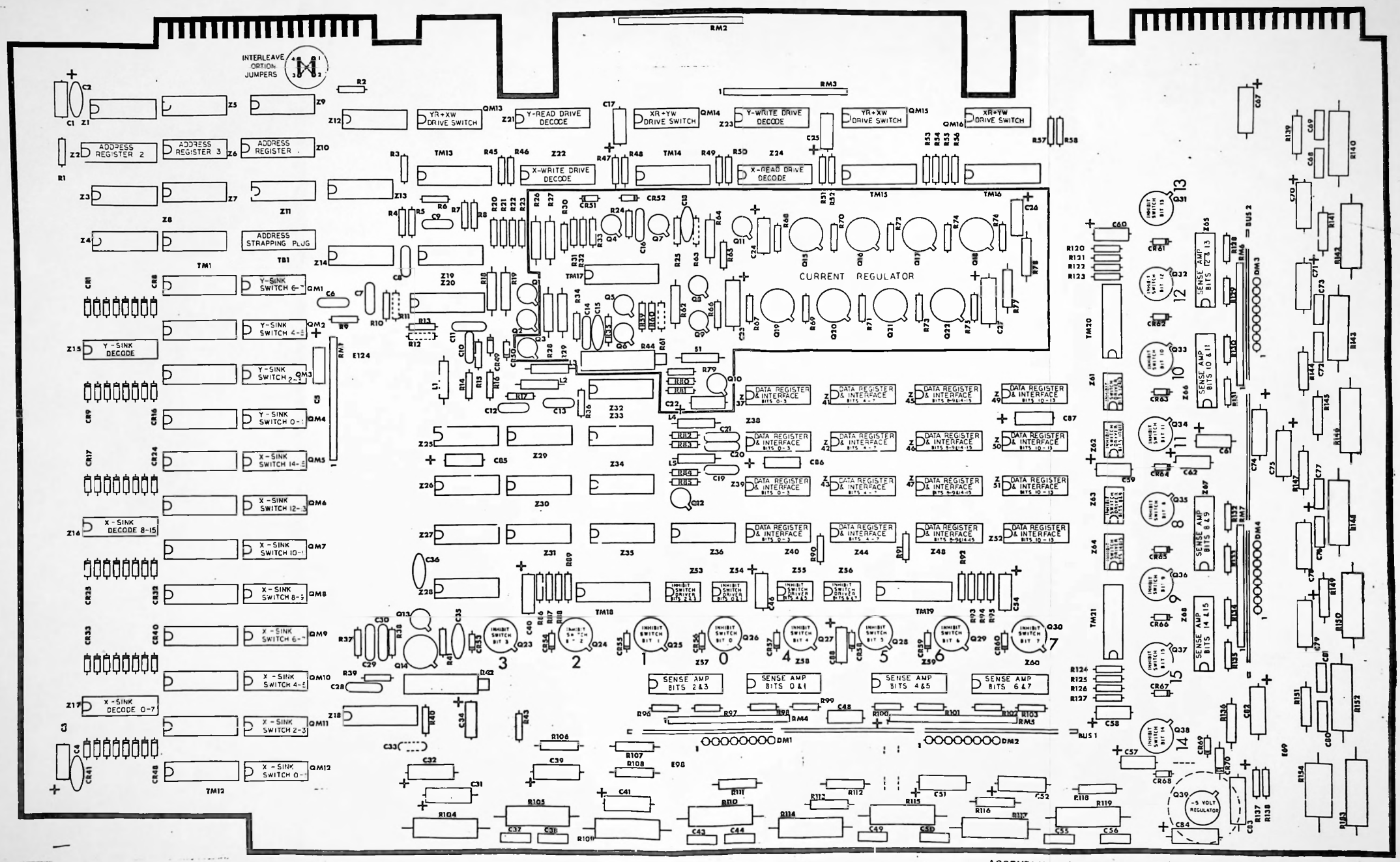
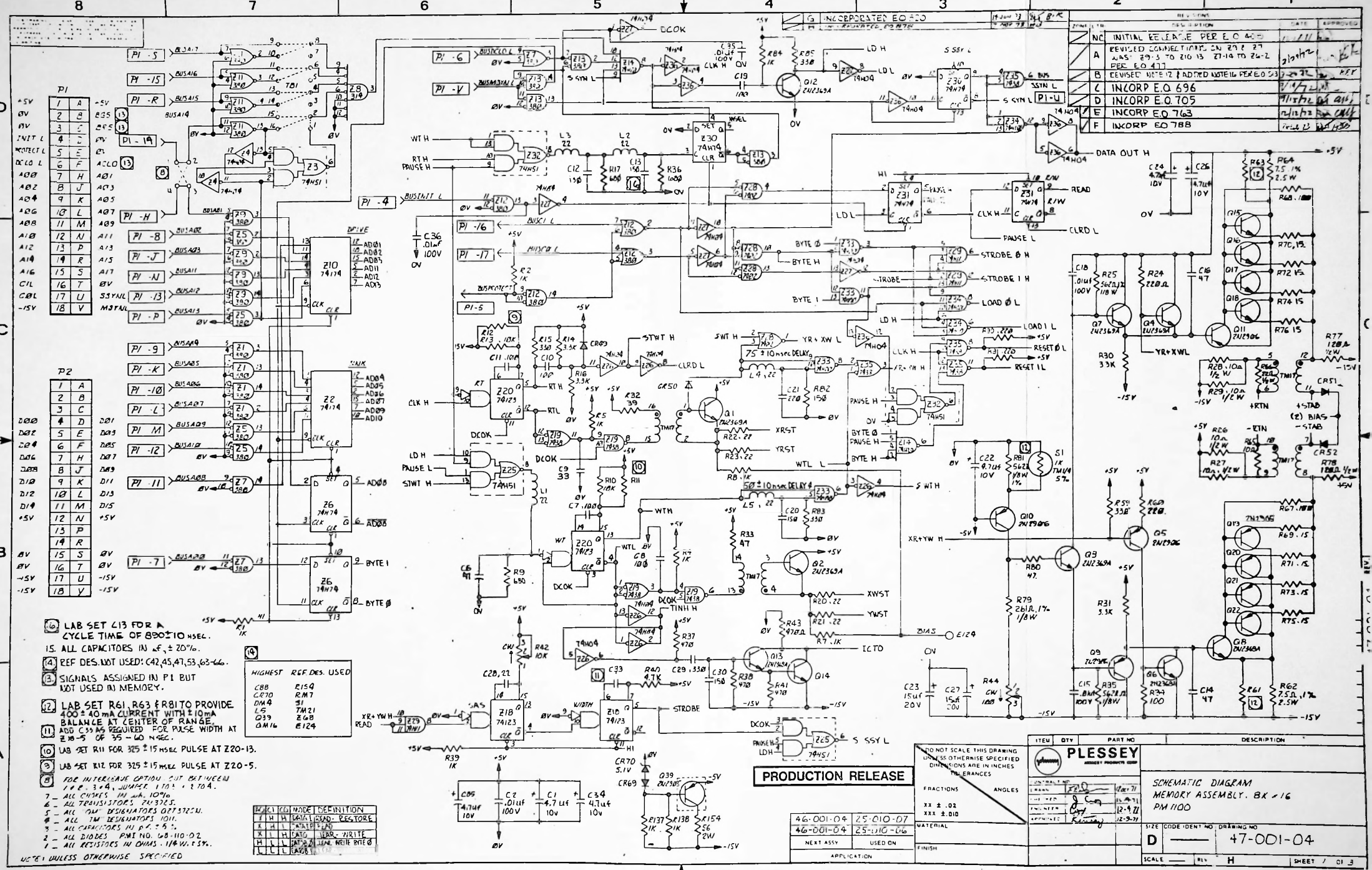
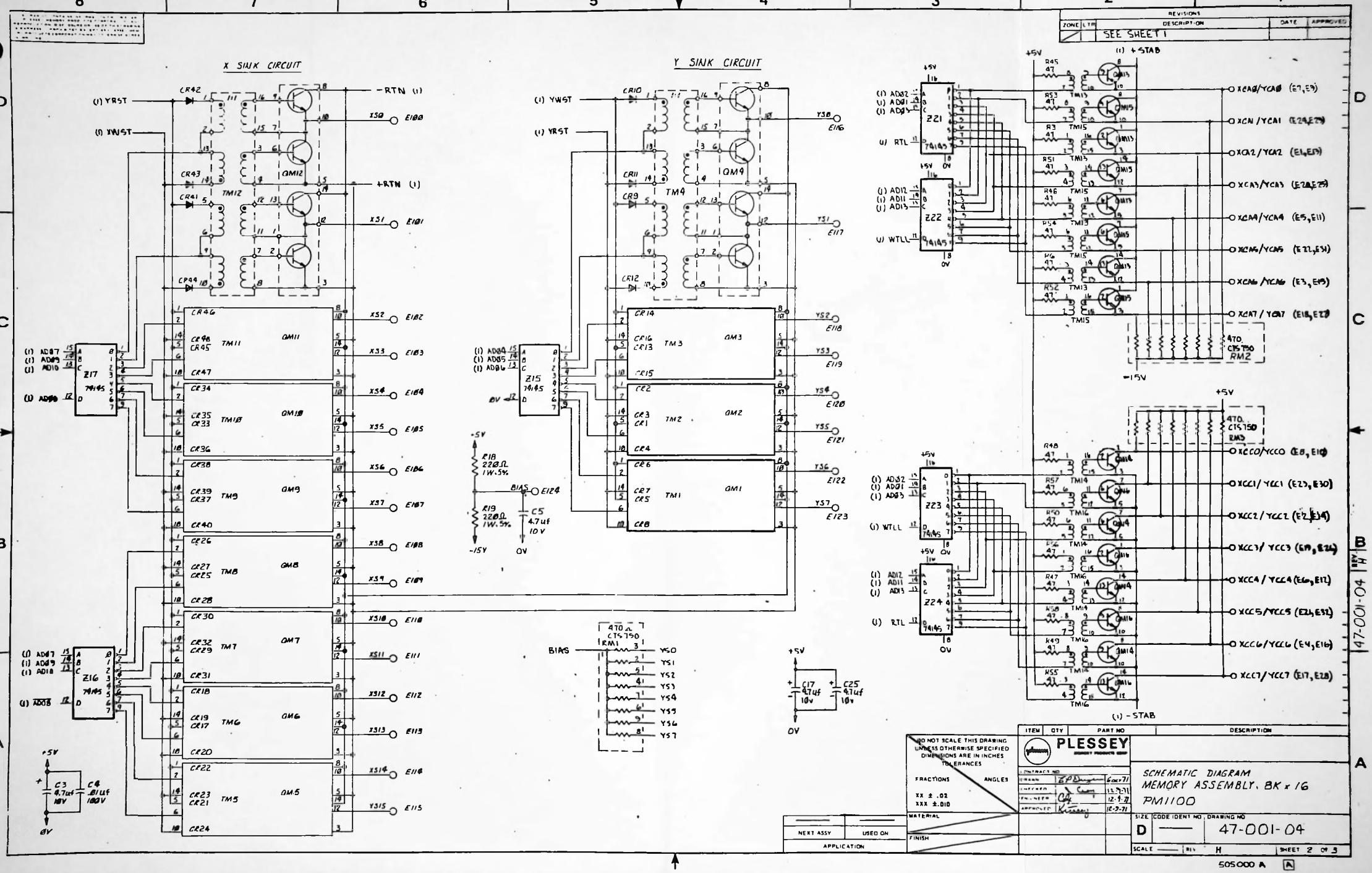
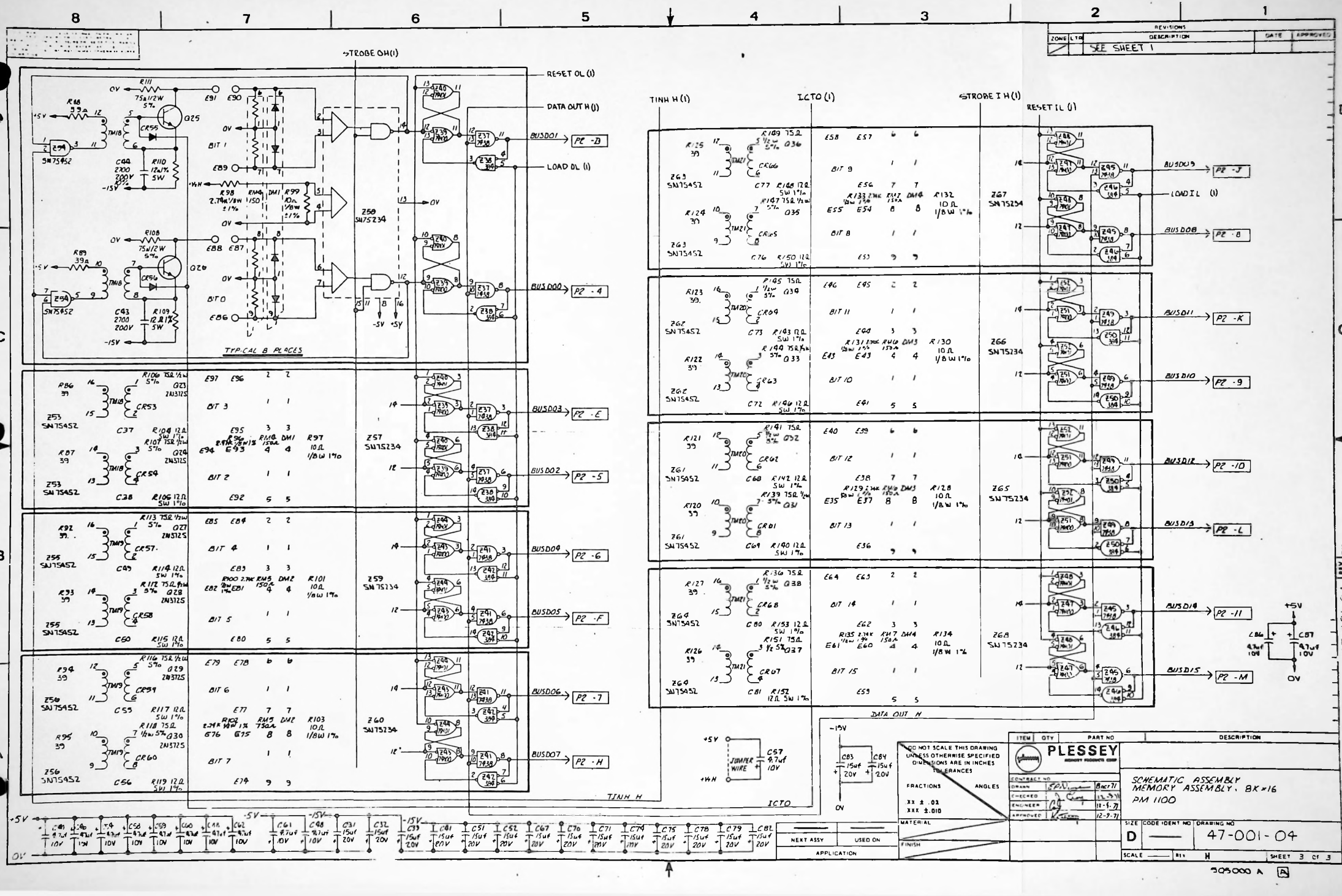


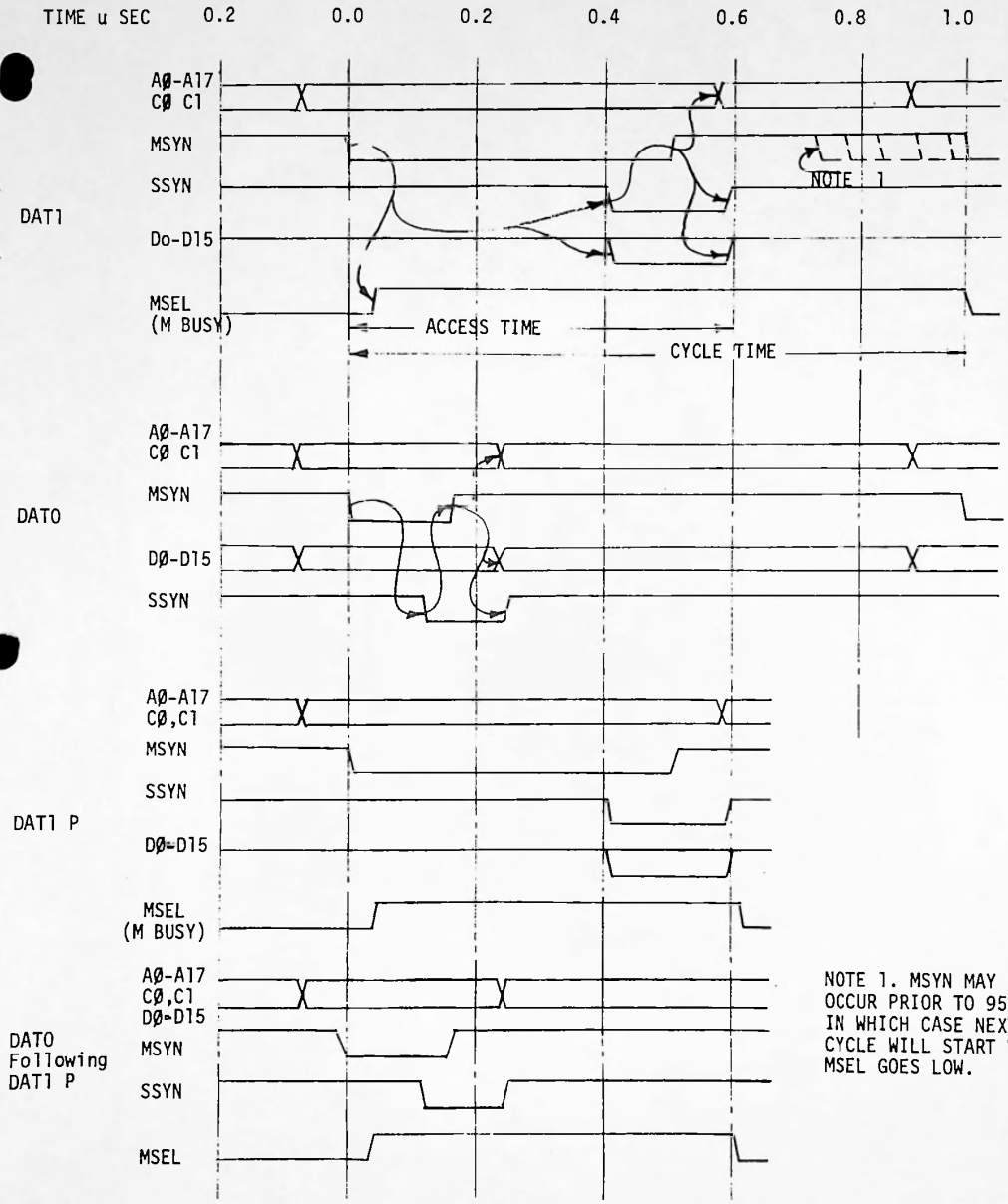
FIGURE 1.

ASSEMBLY DRAWING PM-1100 (8Kx16)
MEMORY SYSTEM


P1
P2
PRODUCTION RELEASE
DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
FRACTIONS
ANGLES
XX ± .02
XXX ± .010
MATERIAL
FINISH
APPLICATION
NEXT ASSY
USED ON
46-001-04
25-010-07
46-001-04
25-016-06
PLESSEY
SCHEMATIC DIAGRAM
MEMORY ASSEMBLY. 8K x 16
PM1100
SIZE
CODE IDENT NO
DRAWING NO
D
47-001-04
SCALE
REV
H
SHEET 1 OF 3
505000 A
A
INCORPORATED E.O 650
INCORP E.O 696
INCORP E.O 705
INCORP E.O 763
INCORP E.O 788
INITIAL RELEASE PER E.O 403
REVISED CONNECTIONS ON Z9 & Z7 WAS: Z9-3 TO Z10 13 Z7-14 TO Z4-2 PER E.O 417
REVISED NOTE 12 & ADDED NOTE 16 PER E.O 513
LAB SET C13 FOR A CYCLE TIME OF 880±10 NSEC.
ALL CAPACITORS IN uF, ± 20%.
REF DES. NOT USED: C42,45,47,53,63-66.
SIGNALS ASSIGNED IN P1 BUT NOT USED IN MEMORY.
LAB SET R61, R63 & R81 TO PROVIDE 400 ± 40 mA CURRENT WITH ± 10 mA BALANCE AT CENTER OF RANGE.
ADD C39 AS REQUIRED FOR PULSE WIDTH AT Z18-5 OF 35-60 NSEC.
LAB SET R11 FOR 325 ± 15 NSEC PULSE AT Z20-13.
LAB SET R12 FOR 325 ± 15 NSEC PULSE AT Z20-5.
FOR INTERLEAVE OPTION CUT BETWEEN 1 & 2, 3 & 4, JUMPER 1 TO 3 & 2 TO 4.
ALL CHOKES IN uh. 10%.
ALL TRANSISTORS 2N3638.
ALL OHM DESIGNATORS OF 3726N.
ALL TM DESIGNATORS 1011.
ALL CAPACITORS IN pf. ± 5%.
ALL DIODES PMI NO. 68-110-02
ALL RESISTORS IN OHMS . 1/4 W. ± 5%.
NOTE: UNLESS OTHERWISE SPECIFIED
HIGHEST REF DES. USED
C88 R154
CR70 RM7
DM4 S1
LS TM21
Q39 Z68
DM16 E124
DRIVE
SINK
BIAS
DATA OUT H
READ
R/W
CLRD L
PAUSE L
LD H
LD L
CLK H
DCOK
STWT H
SWT H
WTH
WTL
RTH
RTL
XRST
YRST
XWST
YWST
ICTO
STROBE
BYTE Ø H
BYTE 1 H
LOAD Ø L
LOAD 1 L
RESET Ø L
RESET 1 L
XR+YW H
XR+YW L
S WTH
S SSY L
S SSYN L
DATA OUT H
+5V
-15V
+RTN
-RTN
+STAB
-STAB
(2) BIAS


X SINK CIRCUIT
Y SINK CIRCUIT
(I) YRST
(I) YWST
-RTN (I)
+RTN (I)
(I) +STAB
(I) -STAB
+5V
-15V
0V
BIAS
R18 220Ω 1W 5%
R19 220Ω 1W 5%
C5 4.7uf 10V
C3 4.7uf 10V
C4 .01uf 100V
C17 4.7uf 10v
C25 4.7uf 10v
470Ω CTS750 RM1
470 CTS750 RM2
470 CTS750 RM3
Z15 74LS5
Z16 74LS5
Z17 74LS5
Z21 74LS5
Z22 74LS5
Z23 74LS5
Z24 74LS5
TM11
TM12
TM13
TM14
TM15
TM16
QM11
QM12
QM13
QM14
QM15
QM16
TM1
TM2
TM3
TM4
TM5
TM6
TM7
TM8
TM9
TM10
QM1
QM2
QM3
QM4
QM5
QM6
QM7
QM8
QM9
QM10
E100
E101
E102
E103
E104
E105
E106
E107
E108
E109
E110
E111
E112
E113
E114
E115
E116
E117
E118
E119
E120
E121
E122
E123
E124
XS0
XS1
XS2
XS3
XS4
XS5
XS6
XS7
XS8
XS9
XS10
XS11
XS12
XS13
XS14
XS15
YS0
YS1
YS2
YS3
YS4
YS5
YS6
YS7
XCA0/YCA0 (E7,E9)
XCA1/YCA1 (E24,E25)
XCA2/YCA2 (E1,E5)
XCA3/YCA3 (E28,E29)
XCA4/YCA4 (E3,E11)
XCA5/YCA5 (E22,E31)
XCA6/YCA6 (E3,E15)
XCA7/YCA7 (E18,E27)
XCC0/YCC0 (E8,E10)
XCC1/YCC1 (E23,E30)
XCC2/YCC2 (E2,E14)
XCC3/YCC3 (E19,E26)
XCC4/YCC4 (E6,E12)
XCC5/YCC5 (E21,E32)
XCC6/YCC6 (E4,E16)
XCC7/YCC7 (E17,E28)
(I) AD07
(I) AD08
(I) AD09
(I) AD10
(I) AD11
(I) AD12
(I) RTL
(I) WTLL
(I) ADD8
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SHEET 1
DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
FRACTIONS ANGLES
XX ± .02
XXX ± .010
ITEM | QTY | PART NO | DESCRIPTION
PLESSEY
MICRO PRODUCTS GMBH
DRAWN EP Dingle 6 Dec 71
CHECKED 13.12.71
ENGINEER 12-12-71
APPROVED 12-12-71
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
SCHEMATIC DIAGRAM
MEMORY ASSEMBLY, 8K x 16
PM1100
SIZE D | CODE IDENT NO | DRAWING NO 47-001-04
SCALE — | REV H | SHEET 2 OF 3
505000 A
47-001-04 REV H


STROBE OH (1)
RESET OL (1)
DATA OUT H (1)
BUSDO1
LOAD OL (1)
BUSDO0
BUSDO3
BUSDO2
BUSDO9
BUSDO5
BUSDO6
BUSDO7
TINH H (1)
ICTO (1)
STROBE I H (1)
RESET IL (1)
BUSDO9
LOAD IL (1)
BUSDO8
BUSDO11
BUSDO10
BUSDO12
BUSDO13
BUSDO14
BUSDO15
TYPICAL 8 PLACES
SEE SHEET 1
PLESSEY
SCHEMATIC ASSEMBLY
MEMORY ASSEMBLY, 8K x16
PM 1100
47-001-04
SHEET 3 OF 3



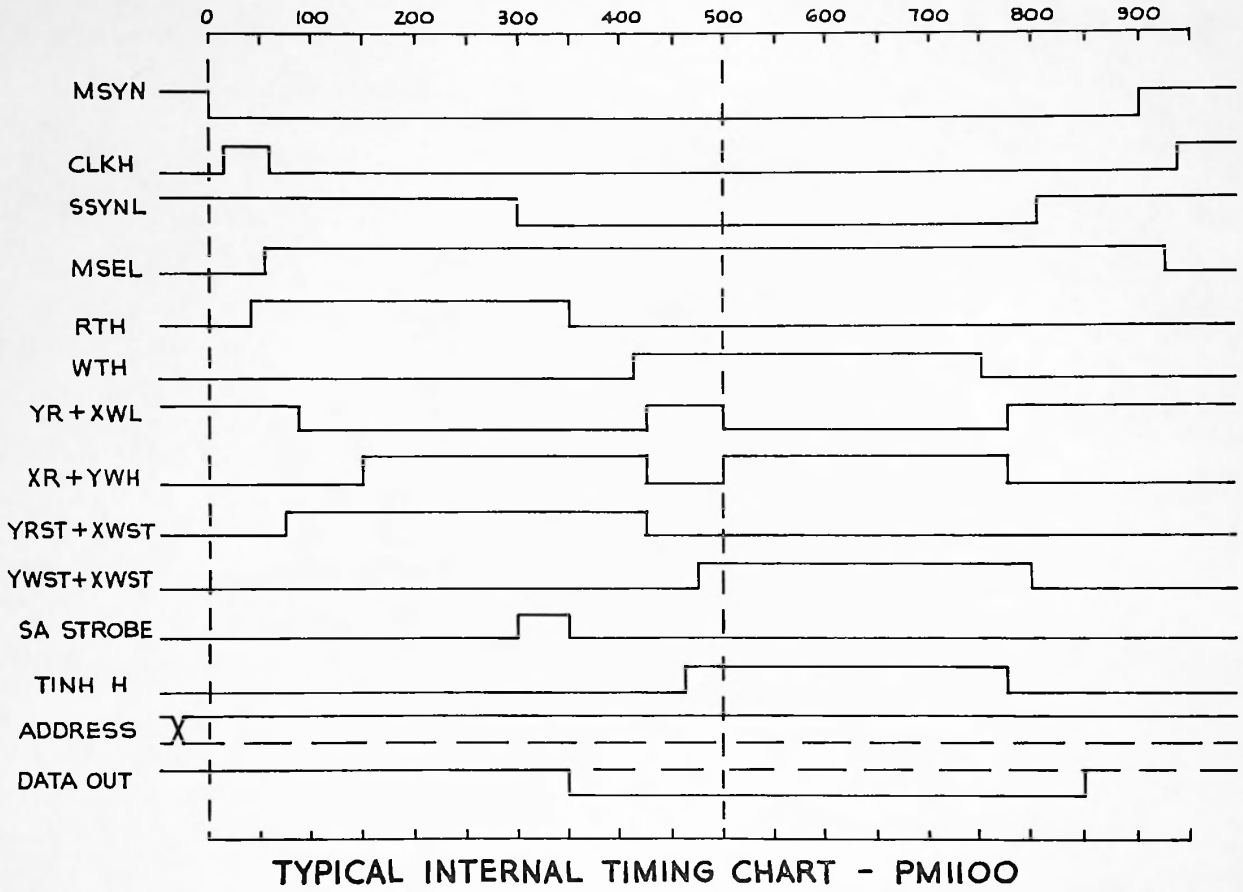
NOTE 1. MSYN MAY OCCUR PRIOR TO 950NSEC IN WHICH CASE NEXT CYCLE WILL START WHEN MSEL GOES LOW.

INTERFACE TIMING DIAGRAM
PM-1100
FIGURE 3.

MODE	COMMAND	CONTROL LINE STATE		
		AØØ	C1	CØ
Read-Restore	DATI	X	Ø	Ø
Read-Half Cycle	DATIP	X	Ø	1
Clear-Write	DATO	X	1	0
Clear-Write Byte 0 Read-Restore Byte 1	DATOB 0	0	1	1
Clear-Write Byte 1 Read-Restore Byte 0	DATOB 1	1	1	1

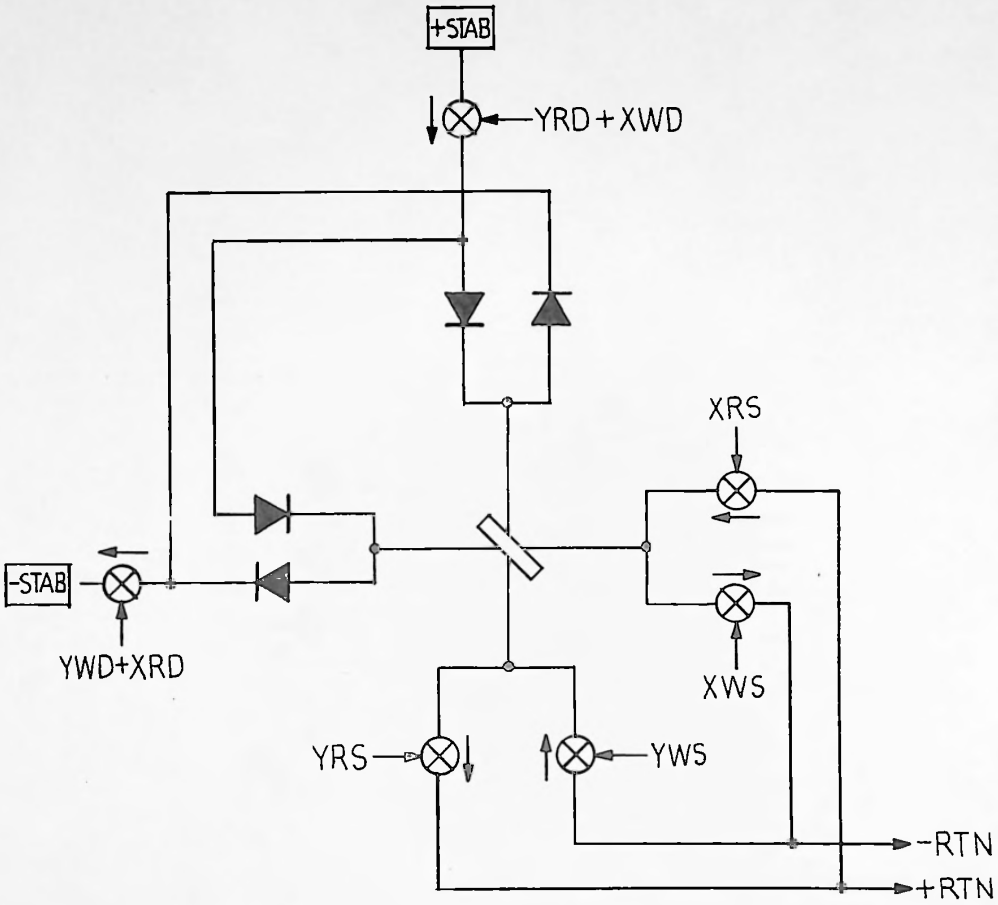
Note: "X" indicates "DON"T CARE" function

FIGURE 4.



TYPICAL INTERNAL TIMING CHART - PM1100

FIGURE 5.



"SHARED DRIVE SCHEME
PM-1100
FIGURE 6.

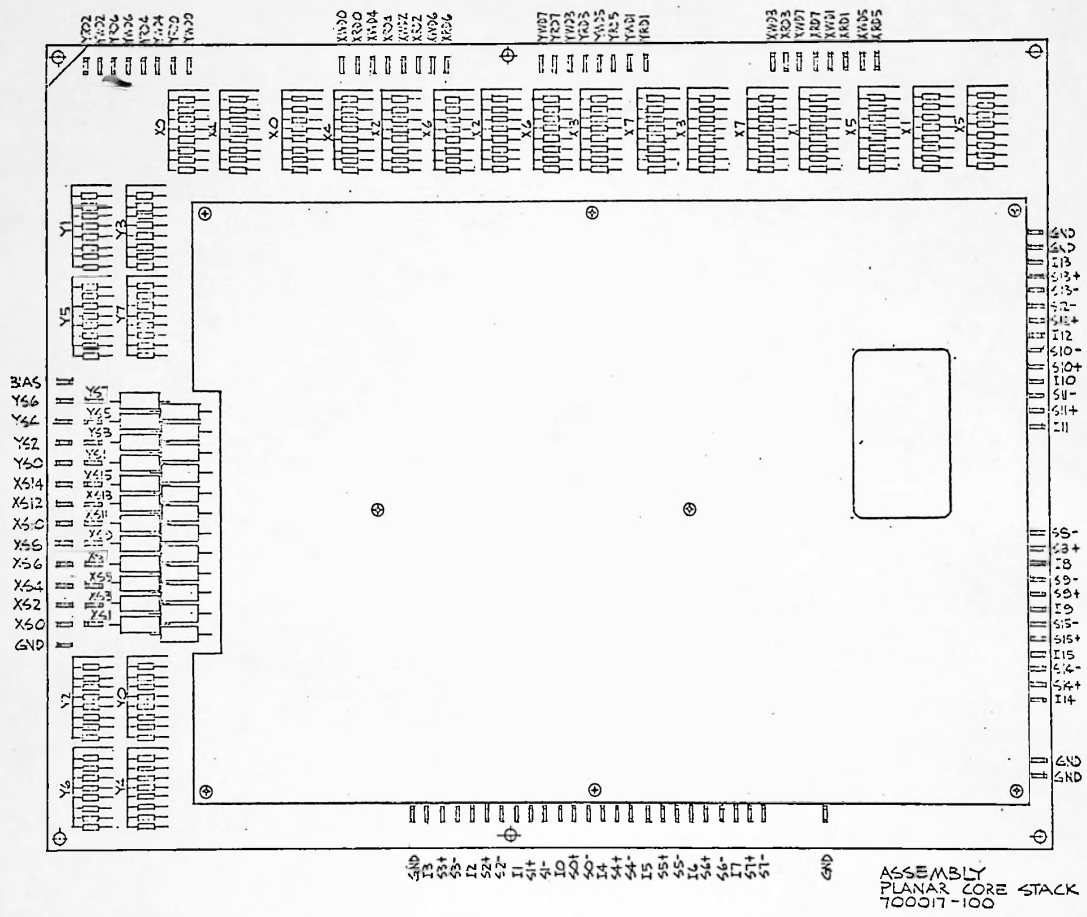
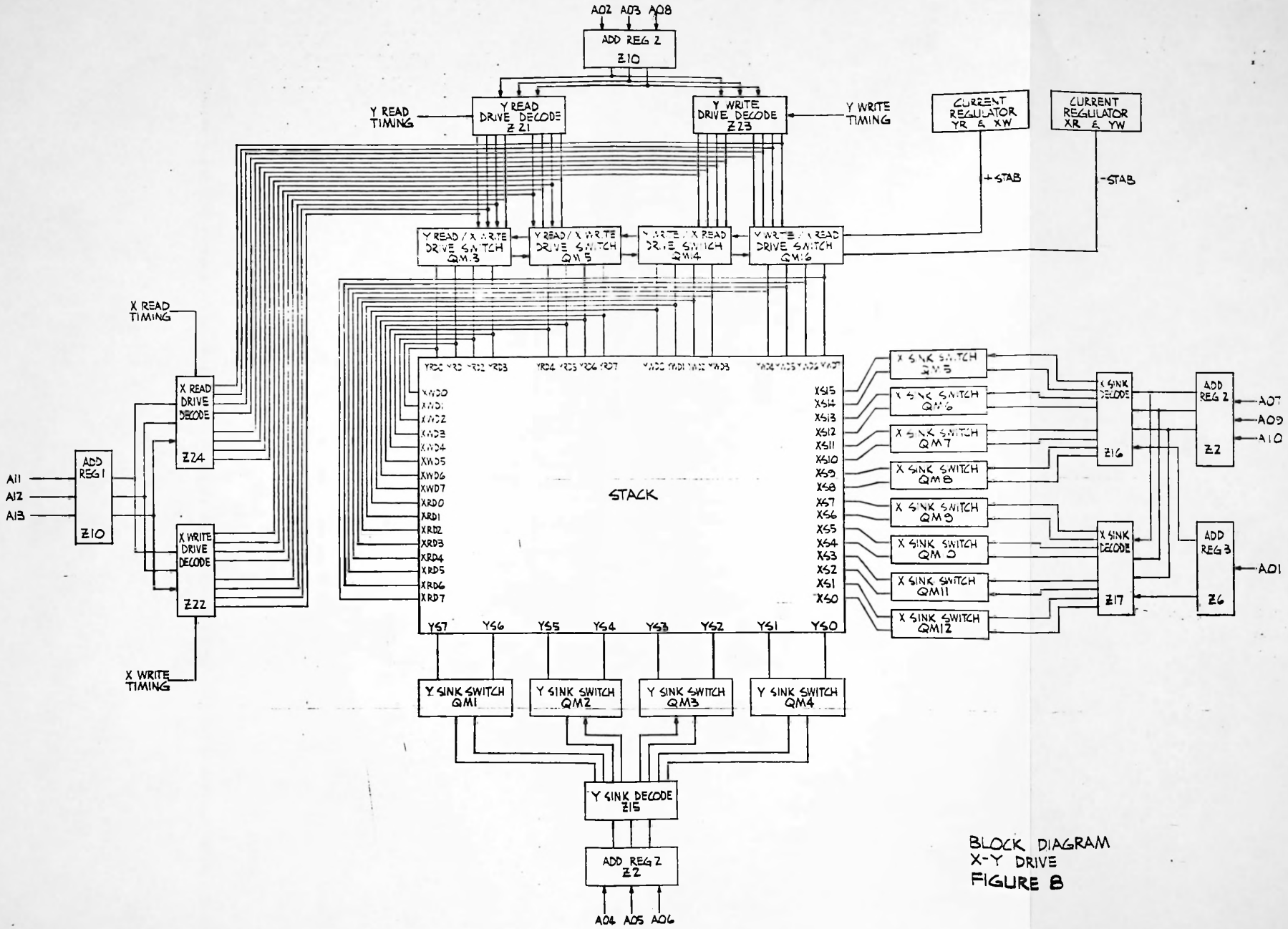


FIGURE 7 .



BLOCK DIAGRAM
X-Y DRIVE
FIGURE 8

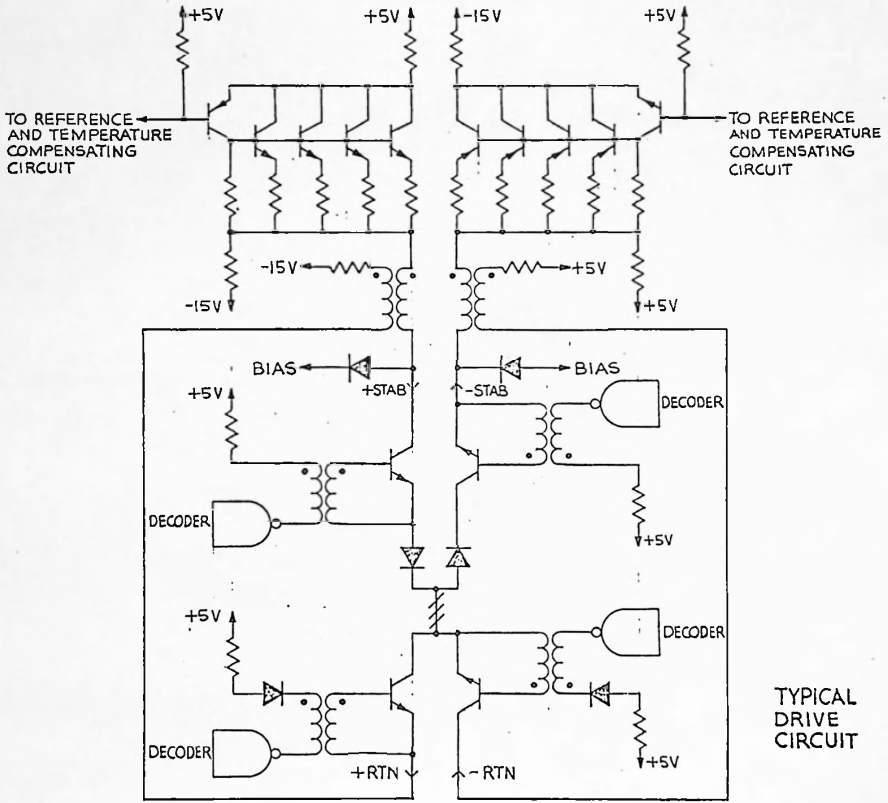
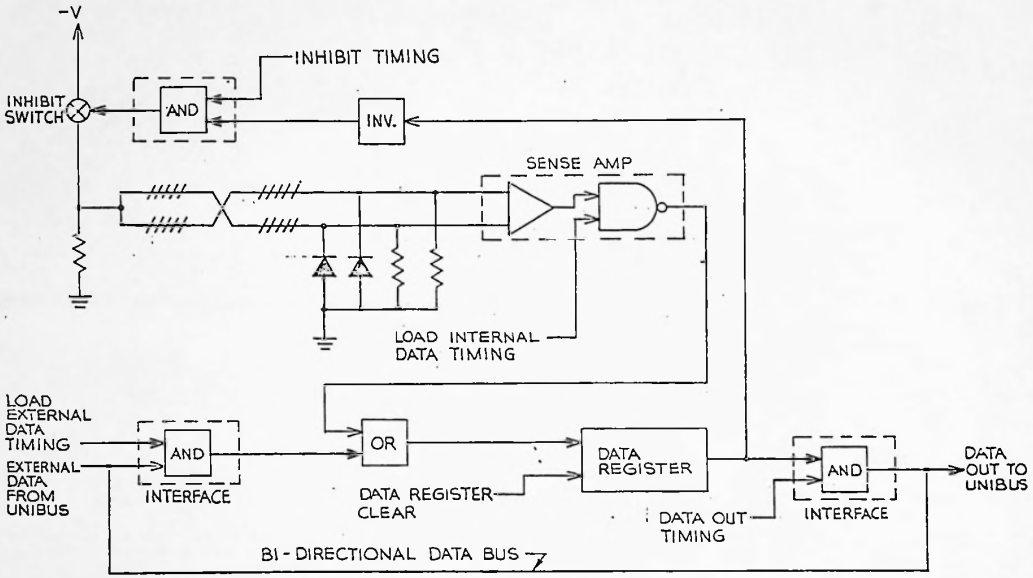
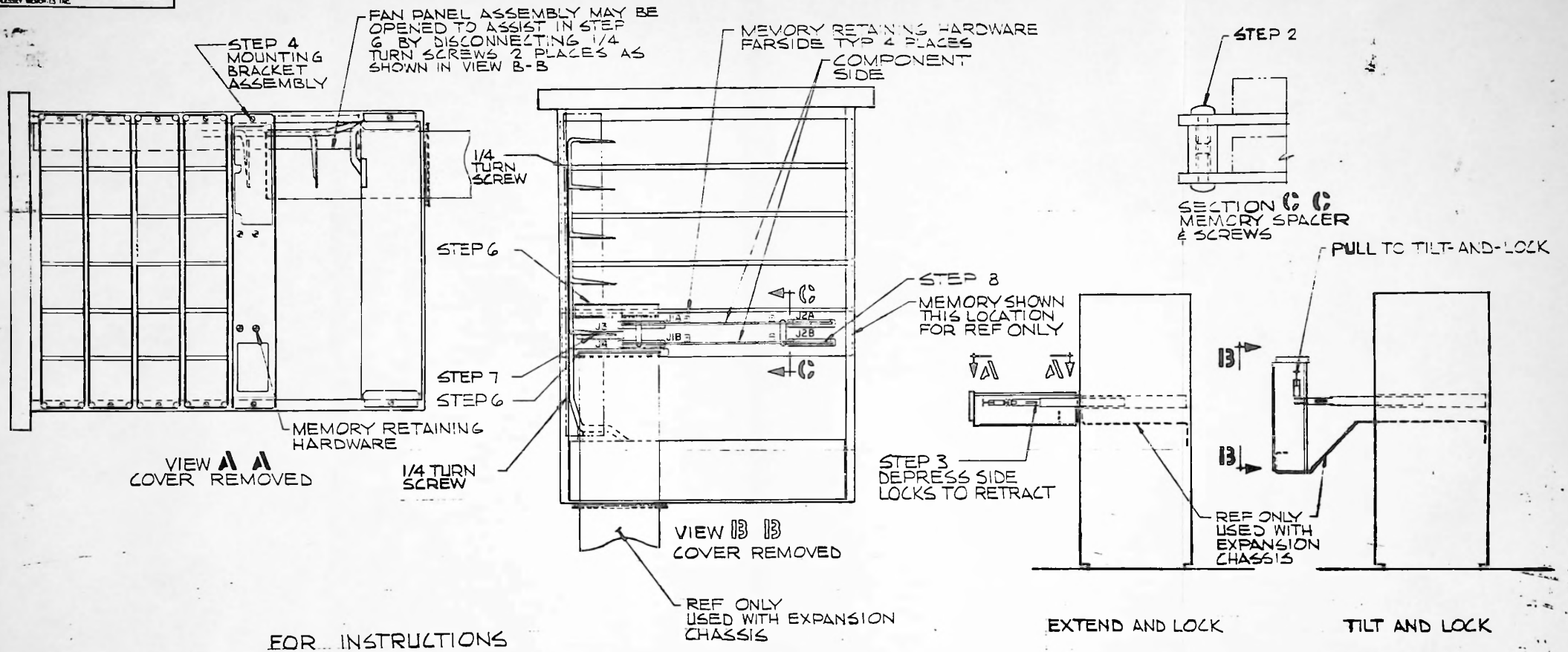

+5V
+5V
-15V
+5V
TO REFERENCE AND TEMPERATURE COMPENSATING CIRCUIT
TO REFERENCE AND TEMPERATURE COMPENSATING CIRCUIT
-15V
+5V
-15V
+5V
BIAS
+STAB
-STAB
BIAS
+5V
DECODER
DECODER
+5V
+5V
DECODER
DECODER
+5V
+RTN
-RTN
TYPICAL DRIVE CIRCUIT

FIGURE 9.



DATA LOOP FOR
A TYPICAL BIT
PM 1100

FIGURE 10.



FOR INSTRUCTIONS
SEE PAGE 10

ZONE LTR	REVISIONS DESCRIPTION	DATE	APPROVED

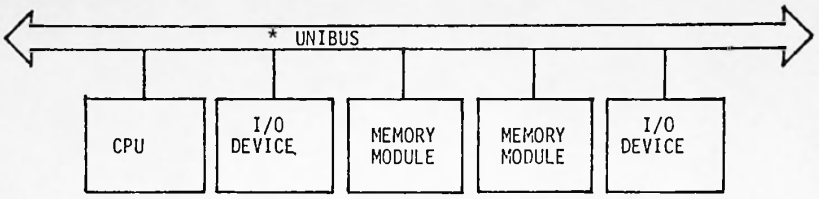
NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST				

PART/ASSY NO. & QTY PER ASSY	DO NOT SCALE DRAWING	CONTRACT NO.	Plessey Memories Incorporated
PART/ASSY REV LTR		DRAWN N. SPENCER 6/1/73	TITLE PM1100 MEMORY INSTALLATION INTO PDP11/20
		CHECK	
		ENGR	
		PROJ. ENGR	
		PROD. DESIGN	
PART NO. NEXT ASSY USED ON APPLICATION		OTHER APPROVALS	SIZE D · CODE IDENT NO. · DWG NO. FIGURE 11 · SCALE · DISTR NO.

APPENDIX A
PDP-11 INTERLEAVE OPTION

1. What is Interleave Option?
2. When can two memories be interleaved?
3. How to excercise the Interleave Option?

What is Interleave Option?



One of the unique features in the architecture of PDP-11 Computer is the way the separate portions that constitute the computer communicate with one another. They communicate via one single set of lines called the Unibus. Naturally, only two devices could communicate via the Unibus at one time. The device that is transmitting information is called the Master of the Unibus and the receiver is the Slave. The Master-Slave relationship is dependent purely on the function performed by the two devices in a given cycle. The master and slave in a cycle may interchange functions in the next cycle. The Central Processor Unit (CPU) which is always considered to be the controller in the conventional computer architectural approaches may become a slave of the unibus in some cycles. The memory is always a slave and cannot issue commands via the unibus.

Each device attached to the Unibus has assigned to it one specific address block. The physical location of a device or its distance of separation has no bearing on the addresses assigned to these devices.

When the device A wants to communicate with the device B, both attached to the unibus, A raises a flag on the unibus indicating to all the other devices on the unibus that it wishes to be the unibus master. The urgency with which this request is granted depends on many factors like device priority etc. When A's request is granted it has complete control of the unibus and A can communicate with any device on the unibus.

The device A now presents the address of the device B to the unibus. All devices on the unibus receive and examine this address information but only the device B responds to the request by sending an acknowledgement. Once A finishes its communication with B, it releases the unibus. The device A or any other device may acquire control of the unibus now.

The memory,which always acts as a slave,takes approximately 950ns to complete a cycle once accessed. Since the memory is self contained in Address Registers, Data Registers and Timing & Control circuitry, it does not have to hang on to the unibus for the entire cycle. Each memory unit attached to the unibus releases the unibus in less than 600ns after it has been accessed. The unibus is now free for exchanging communications between devices but the memory accessed last is still running and will not respond to a request on the unibus for another 350ns (or more) until it completes its internal cycling.

* Unibus is a registered trade mark of Digital Equipment Corporation.

Assume a fast I/O device A is reading out contigious locations in the memory B. A accesses B and receives the data stored in this location in 400ns. B releases the unibus in 600ns but is not ready for A to read the next address location for another 350ns. Since A has to read the next address in this memory it has no alternative but to wait for 350ns until the memory completes its cycle.

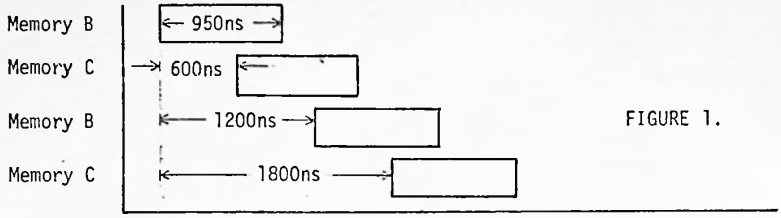


FIGURE 1.

This situation would have been different if the next address happened to be located in a different memory module C. C is not cycling and is ready to accept a request anytime. Thus A accesses C immediately the unibus is released by B. B keeps cycling for another 350ns and will be ready to accept a request by the time C releases the unibus. Thus if B and C are interleaved, i.e. B has all odd locations and C the even locations in an address block or vice versa, a device could be reading or writing data in memory at 600ns cycle time. The device which would take 3 minutes to access an address block without interleave will take only 2 minutes if that address block is interleaved !

When can two memories be interleaved?

Since one memory carries all the odd address locations and the other all the even address locations when interleaved within an address block, only two equal capacity memories can be interleaved. Following table lists all the possible combinations of DEC MM-11F and PM-1100 memories which could be interleaved. It should be emphasized that no variation from this table could be implemented. (DEC MM-11E Memory is not designed for interleave operation)

INTERLEAVE

ADDRESS BLOCK SIZE	MEMORY COMBINATION	STARTING ADDRESS FOR INTERLEAVED ADDRESS BLOCK
8K	Two DEC MM-11F	0, 8K, 16K, 24K etc.
16K	Two PM 1100	0, 16K, 32K, 48K etc.
16K	One PM 1100 & Two DEC MM-11F	0, 16K, 32K, 48K etc.

How to excercise the interleave option?

Figure 2 gives the details on excercising the interleave option in all the possible combinations presently applicable. When interleaving the DEC MM-11F memories among themselves or with PM 1100 memories jumper changes are necessary on the M 1091 Memory Service Select PCB located at B-2 on the MM-11F modules. The required positions of jumpers are shown on Figure 2. Whenever a PM 1100 memory is interleaved the Interleave Jumpers must be placed as shown in Figure 4, i.e. jumpers across 1 & 3 and 2 and 4 (Any connection between 1 & 2 and 3 & 4 shall be removed).

ADDRESS BLOCK	INTERLEAVED MEMORIES	DEC MM-11F 4Kx16 MODULE									PM1100 8Kx16 MODULE
		JUMPER LOCATIONS ON M1091 PCB AT LOCATION B-2									ADDRESS STRAPPING PLUG ON TS 1
		Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 1	Bit 1 Or 13	
0-8K	DEC MM-11F (4K)	0	0	0	0	A			D	0	NA
	DEC MM-11F (4K)	0	0	0	0	A			D	1	
8K-16K	DEC MM-11F (4K)	0	0	0	1	A			D	0	NA
	DEC MM-11F	0	0	0	1	A			D	1	
16K-24K	DEC MM-11-11F	0	0	1	0	A			D	0	NA
	DEC MM-11F	0	0	1	0	A			D	1	
24K-32K	DEC MM-11F	0	0	1	1	A			D	0	NA
	DEC MM-11F	0	0	1	1	A			D	1	
0-16K	DEC MM-11F	See Figure 3A									NA
	DEC MM-11F	See Figure 3B									NA
	PM 1100	N/A									700066-105
0-16K	PM 1100	N/A									700066-105
	PM 1100	N/A									700066-107
16K-32K	PM 1100	N/A									700066-108
	PM 1100	N/A									700066-109

* Basic PDP-11 Computer can address only 28K of memory.

FIGURE 2

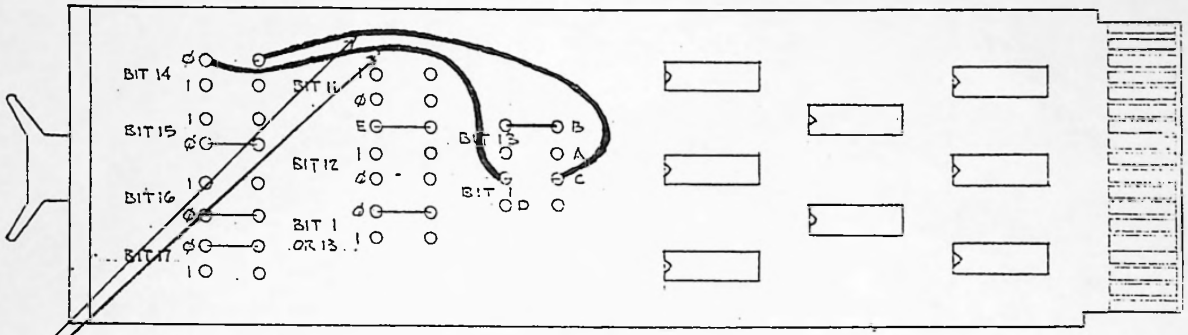


FIGURE 3-A

Add Four Insulated Jumpers As Shown

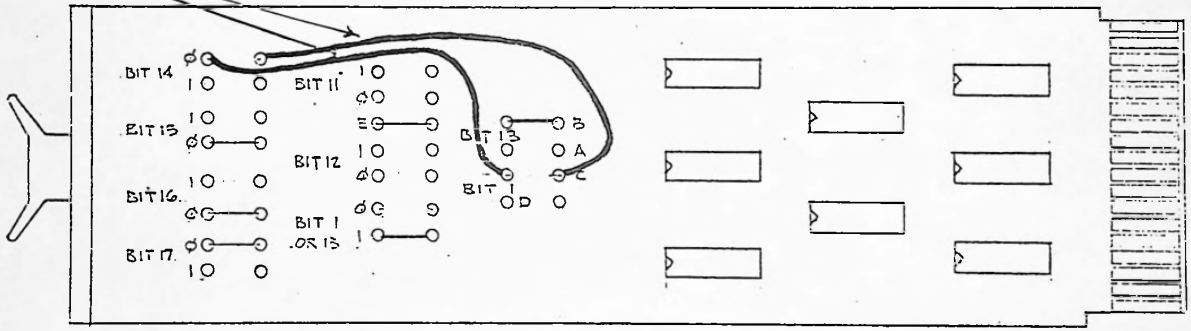


FIGURE 3-B

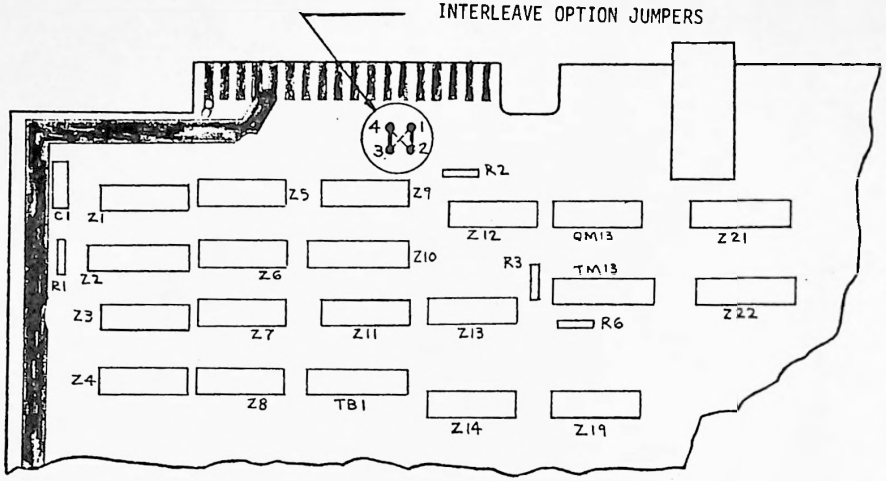

INTERLEAVE OPTION JUMPERS
4
1
3
2
R2
C1
Z1
Z5
Z9
Z12
QM13
Z21
R1
Z2
Z6
Z10
R3
TM13
Z3
Z7
Z11
Z13
R6
Z22
Z4
Z8
TB1
Z14
Z19

FIGURE 4.

* CAPACITY	PART NUMBER	JUMPER LOCATION						
		1-2	16-2	15-2	13-4	14-4	12-6	10-8
0 - 8K	700066-105		X			X	X	X
4K - 12K	700066-106	X				X	X	X
8K - 16K	700066-107			X		X	X	X
16K - 24K	700066-108		X		X		X	X
24K - 32K	700066-109			X	X		X	X

* These capacities are valid for non-Interleave Operation only.

ADDRESS STRAPPING PLUG - PM 1100

FIGURE 5.

Plessey Microsystems, 1674 McGaw Avenue, Irvine, CA 92714 • Tel: (714) 540-9945.